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# **1** INTRODUCTION

The purpose of this document is to define expectations, specifications, contexts, and provide additional details that are consistent requirements among IF Engineering products. This document is intended to be read by IFE suppliers.

Suppliers providing PCB fabrication services and Metalwork Fabrication are responsible for sections indicated in the chart below.

Section Number	Section Title	PCB Supplier Requirement	Metalwork Fabrication Requirement
1	Introduction	Yes	Yes
2	Related Documents	Yes	Yes
3	Requirement Hierarchy	Yes	Yes
4	PCB Fabrication Requirements	Yes	No
5	Metalwork Fabrication Requirements	No	Yes
6	Deviations from this Document	Yes	Yes

# 2 RELATED DOCUMENTS

The following is a related document

WI-1002 Section HSPPD Quality Procedures Manual – Handling, Storage, Preservation, Packaging & Delivery of Manufactured Product

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# **3** REQUIREMENT HIERARCHY

This document intends to specify relevant requirements and specifications in order to fabricate raw printed circuit boards (PCBs). Unavoidably, there are occasions where IFE Requirements are more stringent than an industry standardized document. See below for requirement clarifications.

# 3.1 HIERARCHY OF REQUIREMENTS - LISTED FROM HIGHEST TO LOWEST ORDER OF

# PRECEDENCE

- 1. IFE Personnel
- 2. IFE Drawing
- 3. IFE Detailed Requirement (from This Document)
- 4. Most stringent specification (Industry Specification or other contained in this document)

# 4 PCB FABRICATION REQUIREMENTS

# 4.1 IPC-6012A FABRICATION SPECIFICATIONS

PCB should be capable of meeting IPC-6012A, Class 2; per IPC-6011 using customer supplied data files.

# 4.2 MATERIAL REQUIREMENTS

# 4.2.1 Dielectric Tolerances

Dimensions shall have a  $\pm$  10% thickness tolerance unless otherwise noted in the fabrication drawing.

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4.2.2	FR4 Dielectric Selection and Nominal Thickness Dimensions are specified in FINISHED thicknesses. Manufacture in accordance with IPC-TM-650 2.4.8 Current revision.	L1	FR4 Dielectric	
	Dielectrics thicknesses specified as TBD (or unspecified) permit variation by fabrication vendor, subject to meeting all other requirements.	L2	FR4 Prepreg	
	<b>Prepreg thicknesses should be accounted</b> for in the stack up and the copper layer to copper layer distance shown on the fabrication	L3	FR4 Core	
	drawing should be maintained.		FR4 Prepreg	
		L4	FR4 Dielectric	
4.2.3	Other Dielectric Selection (Proprietary Materials) Nominal Thickness This section includes, but is not limited to Rogers and Taconic's	L1	Rogers / Taconics / Specialty	
	materials. Dimensions are thicknesses of specified material as		Prepreg	
	specified in manufacturer datasheets (before press and lamination if relevant).	L2	Core 21	
	Prepregs are NOT included in the drawing thicknesses and are	L3		
	typically not specified. A prepreg compatible with the specified		Prepreg	
	material in accordance with vendor experience, or manufacturer's specification.		Rogers / Taconics / Specialty	
	Stack up structures may vary from the picture.	L4	_	

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#### 4.2.4 Copper Thicknesses

When copper thicknesses are specified in ounces/ $ft^2$ , thicknesses are to be as follows: 0.5oz = 0.7mil, 1.0oz = 1.4mil, and so forth.

#### 4.2.5 Surface Finish Requirements

4.2.5.1 Electroless Nickel Immersion Gold (ENIG) Plating (Normal) ENIG shall be in accordance with IPC-4552 Current Revision.

ENIG Requirement (Normal): Thickness 0.025-0.13um (1-5u-inch) Au Over 3-6um (118-236u-inch) Ni

# 4.2.5.2 Thin Electroless Nickel Immersion Gold (Thin ENIG) Option (when specifically requested)

Thin ENIG Requirement (when specifically requested by IFE): Thickness 0.05-0.13um (2-5u-inch) Au Over 1.5-3um (59-118u-inch) Ni

#### 4.2.5.3 Other Finishes

Other types of plating specified may include HASL (Non-RoHS), RoHS HAL Tin, Immersion Tin, and Immersion Silver, and will be indicated on fabrication drawing when needed.

# 4.3 CAD ITEMS

#### 4.3.1 Design Package

Board fabrication files are packaged in a single compressed zip file.

#### 4.3.2 CAD File List

Boards will have a design file associated with each design layer that shall be used for fabrication. Irrelevant layers may not be present when data is not required for them (such as no Bottom Silkscreen, or no inner layer, or no solder mask).

Fabrication Layer

- O Overall board size and thickness
- o Stack up including dielectric materials and thicknesses, and copper weights.

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- Drill chart. All holes are plated unless specified as non-plated holes.
- Drill Layer (Plated Holes)
- Drill Layer (Unplated Holes)
- Copper Layer Top (Note 1)
- Copper Layer Bottom (Note 1)
- Copper Layer Inner (Notes 1 & 2)
- Solder Mask Top (Note 2)
- Solder Mask Bottom (Note 2)
- Silkscreen Top (Note 2)
- Silkscreen Bottom (Note 2)

Note 1: Possibilities include one file, or multiple files which need to be merged.

Note 2: This file is included when it is relevant, and as such will have an inference in the fabrication drawing. It may not be included in other cases. For example, if no inner layers exist, subsequently no inference in the fabrication drawing exists, and therefore no Copper Inner Layer Gerber file exists.

#### 4.3.3 CAD Imperial Units

Boards are designed in thousandths of an inch, and will also be referred to as "mils".

#### 4.3.4 CAD File Output Formats

Gerber files are in RS-274-X formats. Units are imperial (inches). Numeric data is in 3 Leading, 5 Trailing Digits. Leading Zeros are suppressed. Coordinates are Absolute. Circular interpolation is set to Full.

#### 4.3.5 Drill Holes

Drill-hole sizes specified on fabrication notes are finished dimensions. Drill size tolerance is  $\pm$  0.003".

Drill-hole position tolerance is  $\pm$  0.003" unless otherwise stated.

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# 4.3.6 Inside Radii

Inside corners with an unspecified radius (or zero radius) in Gerber files are to have a maximum radius of  $0.020^{\circ}$ . Radii specified in drawing, whether smaller or larger than  $0.020^{\circ}$  shall have radius tolerance  $\pm 10\%$ .

#### 4.3.7 Gerber Modification

Gerber files or data are not to be modified in any manner without direction from an IFE representative.

# 4.4 MANUFACTURING

#### 4.4.1 Mechanical

Dimension features and specifications are specified for reference. Gerber data should be used for board

#### 4.4.1.1 Board Dimension

Gerber data shall be used when determining nominal manufacturing dimensions. Board dimensions are specified in the Board Fabrication Layer and are for reference only.

Note any edge finger plating details on drawing.

# 4.4.1.2 Overall Board Thickness

Board thickness tolerance is  $\pm$  10%.

#### 4.4.2 Stackups

Board layer stackups shall be in accordance with specification on fabrication drawing. The Layer order, or layer sequence, shall not be modified without specific instruction from IF Engineering. See **Material Requirements**, Section **4.2** for dielectric specifications.

# 4.4.3 Annular Ring

Minimum annular ring shall be in accordance with IPC-6012 Class 2 Current Revision. Plate Holes with a minimum of 0.001" plating if not otherwise specified in drawing.

#### 4.4.4 Registration

Board registration must be no more than 0.003" in X or Y direction, from one layer to any other one layer.

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4.4.5 Drill Holes (see Drill Holes Section 4.3.5) See Drill Holes Section 4.3.5.

#### 4.4.6 Silkscreen

Silkscreen shall be **white** color if not specified in drawing. Vendor to use an epoxy-based, nonconductive ink. Silkscreen shall be trimmed from all solderable surfaces.

#### 4.4.7 Solder Mask

Liquid Photo Imageable (LPI) Solder Mask with Solder Mask over Bare Copper (SMOBC) technology shall be used per IPC-SM-840 Current Revision. Green solder mask is preferred unless otherwise specified in fabrication layer.

4.4.8 Via Tenting and Via Plugging (only when indicated on drawing) Via tenting and plugging shall be in accordance with the requirements below, and shall ONLY be required when indicated on drawing.

Via solder mask plug and solder mask overprint (for vias 0.020" diameter and smaller): vias containing solder mask coverage in the CAD files shall be filled with an approved solder mask and over-coated with solder mask. Final via shall be no less than 60% coverage. Final protrusion height of solder mask plug above vias shall not exceed 2.5mil. Trim solder mask off of overlapping component pad.

4.4.9 Edge Plating (when indicated on drawing)

It is permissible to omit edge plating in areas where array rail tabs are specified, when array drawings are included.

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# 4.5 PANELIZING INFORMATION

This section contains information helpful to IFE and PCB fabrication suppliers. Its purpose is to provide information that will aid in panel size selection. It is most preferable to deliver the largest size panel compatible with Table 1, which is capable of being processed at IFE.

The limitation when selecting larger panels can be determined in this section between the two tables. As implied by the table, smaller panel sizes are acceptable, especially if material waste is less, if material waste has been reasonably minimized, or if instruction has been given by IFE in terms of size dimension, cost, or specified explicitly.

# 4.5.1 CAD Submittal

When panel layout is performed by PCB Fabrication Supplier as requested by IFE personnel, submittal of panel layout information is required prior to fabrication delivery.

Acceptable CAD is considered electronic files in Gerber format, DWG, DXF, indicating panel fiducials, spacing and board to panel attachment detail.

	Panel Dimensions					IFE Capa	bilities		
Precedence	Length	Width		Stenciling	Pick & Place	Reflow Oven	Automated Stenciling	AOI	Depanelizing CNC
1	12.00	9.00		Yes	Yes	Yes	Yes	Yes	Yes
2	14.00	9.75		Yes	Yes	Yes	Yes	Yes	No
3	15.75	11.50		Yes	Yes	Yes	Yes	No	No
4	19.00	11.50		Yes	Yes	Yes	No	No	No

# 4.5.2 Preferred Maximum Panel Sizes

Table 1. Preferred Maximum Panel Sizes. Dimensions are in inches.

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# 4.5.3 Panel Size Equipment Limitations and Capabilities

Description	Ма	ах	Mi	n
	Length	Width	Length	Width
Stencil	24.00	29.00		-
Stencil Printer	15.75	15.75	0	-
Pick & Place	19.00	11.50	NV V	1.75
Conveyor 1	16.00	16.00	-	1.50
Reflow Oven	<u> </u>	17.25	-	5.25
Conveyor 2	20.00	18.50	-	1.75
AOI	14.00	9.75	-	2.00

Table 2. Panel Size Limitations of Equipment. Dimensions are in inches.

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#### 4.5.4 Preferred Mouse Bites

Mouse Bites are preferred technique by IFE when panelizing a PCB. The mouse bite details are below.

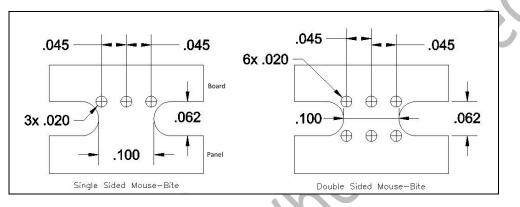
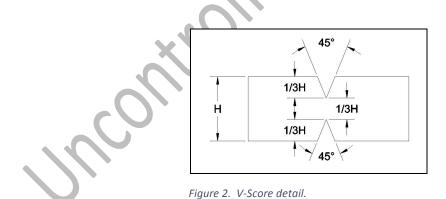


Figure 1. Mouse Bite detail.

#### 4.5.5 V-Score

V-Scores may be needed according to the fabrication drawing or requested by IFE Personnel. The preferred v-score details are below.



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# 4.6 QUALITY REQUIREMENTS

Product shall be in accordance with IPC-A-600, Class 2 Current Revision, Acceptability of PCBs.

Product shall be **capable** of meeting **IPC-6012 Class 2 Current Revision**, Qualification and Performance for Rigid PCBs. No coupons are required.

#### 4.6.1 Electrical Testing

**Note, Many IFE PCB jobs are 2 layer boards that do not require electrical testing.** However, electrical bare board testing is required in either of the following cases

- Complex PCBs PCBs with 100 or more nets & any traces 20mils or thinner & any single component with a pitch of 0.100" or finer.
- Drawing Requirements PCBs with fabrication drawings that indicate electrical test requirements

# 4.6.1.1 Test Criteria

Use this criteria when electrical testing is required.

- IPC 9252A Test Level C (Class 3)
- 100% Electrical net testing.
- Isolation Meg Ohms: not less than 10 Mega Ohms
- Continuity Testing (Normal): not greater than 10 Ohms at 40volts.
  Supplier may alternatively or voluntarily test up to 250volts at their discretion.

High Voltage Continuity Testing (Special): if high voltage testing is specified on drawing, test is to be performed at 10 ohms 250 volts.

# 4.6.2 Mechanical Criteria

Board warp: 1%, per IPC-TM-650; 2.4.22

# 4.6.3 Marking

Marking shall be etched into copper layers.

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#### 4.6.3.1 Lot Code

Lot Code indicating last 2 digits of the active calendar year of start of manufacture, and 2 digits indicating week of the calendar year.

#### 4.6.3.2 Manufacturer Marking

PCBs are required to have a unique recognizable marking indicating manufacturer of the raw PCB

# 4.7 PCB DELIVERABLE REQUIREMENTS

Deliverable requirements are specified in purchase order. Typical items are listed below and are for reference. Additional documents may be necessary.

# 4.7.1 Raw PCBs as specified in purchase order

#### 4.7.2 Solder Sample

A solder sample representative of the relevant lot of PCBs.

# 4.7.3 Test Results (When Applicable)

Test results for relevant PCBs that need or have electrical test specified.

# 4.7.4 Packing and Shipping

For packing and shipping requirements see document WI-1002.

# 5 METALWORK FABRICATION REQUIREMENTS

# 5.1 PART MARKING

# 5.1.1 Part Marking Criteria

Parts are required to be marked in any of 2 cases below.

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#### 5.1.1.1 CPT-XXX-28XX or CPT-XXX-29XX PART NUMBERS

Parts that meet the P/N criteria above are subject to the Part Marking Requirements below.

#### 5.1.1.2 XXX-XXX-28X PART NUMBERS or XXX-XXX-29X

Parts that **indicate a part marking location AND** meet the P/N criteria above are subject to the Part Marking Requirements below.

Note: XXX-XXX-28X Parts that do not indicate a marking location are not required to have marking.

#### 5.1.2 Marking Requirements

#### 5.1.2.1 Part Number

Parts shall indicate IFE Part Number and revision indicated on drawing and Purchase Order.

It is permissible to have minor inconsistent spacing of characters to a reasonable degree based on tooling such as mechanical stamping or rubber stamping, so long as all characters of the part number and revision are present and legible.

#### 5.1.2.2 Small Parts

When area to be marked is less than 2" in length, the following options are permissible.

- It is permissible to spread part numbering and revision across multiple lines to accommodate tooling, or physical area of part.
- It is permissible to mark only "Rev" followed by the revision number / letter.
- It is permissible to mark only the revision number / letter
- It is permissible to shrink the text size such that magnification no greater than 4x is required for human inspection.

# 5.1.2.3 Post Surface Finishes

Parts that require surface finishing as part of the Purchase Order, such as paint, electroplating, or iridite, shall be either visible or marked after the last surface finish operation is completed.

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#### 5.1.2.4 Acceptable Technologies (Permanent)

Marking shall be permanent and may use any of the following technologies listed, in order of preference (non-inclusive). CNC or machine methods are preferred, however manual methods are also permissible. IFE may accept new technologies not on this list. All marking shall be legible.

- Engraving
- Laser Etching
- Mechanical Stamping
- Rubber Stamping or use of indelible ink designed or proven to resist alcohol, degreasers, cleaning fluids, trichloroethylene, and soap and water.

#### 5.1.2.5 Part Marking Location (Important!)

Location is described according to part number format below where 'X' represents any numeric digit.

- CPT-XXX-16XX PANEL, FRONT OR REAR Mark Far side surface of main view in Sheet 1.
- CPT-XXX-16XX (Other) Marking location shall be based on vendor capabilities unless otherwise indicated on Drawing.
- XXX-XXX-16X Mark ONLY if Location is indicated in Drawing. DO NOT MARK if no location is indicated.

# 5.2 PACKING AND SHIPPING

For packing and shipping requirements see document WI-1002.

# 6 DEVIATIONS FROM THIS DOCUMENT

Refer to Section 3, Requirement Hierarchy, for deviations from this document. IF Engineering Personnel shall be conferred with if there is a questionable item, or seemingly conflicting requirements.

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This section is for reference only. Change descriptions below prior to the previous revision of the current document, may be progressively condensed and summarized.

Revision		Change	Date
-	Prelim		10/4/2016
-	Prelim		11/15/2016
-	Prelim	4.1 Change "Fabricate PCB in accordance with IPC-6012A" To	11/21/2016
		"PCB should be capable of meeting IPC-6012A"	
		4.2.4 Corrected "Ounces / sq. ft." from "Ounces / Sq. in."	
		4.5 Change "in accordance with IPC-6012"to "be capable of meeting IPC-6012"	
	~	4.5 Add "No coupons required."	
	<u>n</u>	4.5.1 Change "Complex PCBs - PCBs with 30 or more nets" to "Complex PCBs - PCBs with 100 or more nets"	
		4.5.1.1 Change FROM	
		4.5.1.1 Test Criteria	
		o 100% Electrical net testing.	

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Revision		Change	Date
		o Continuity Ohms: not greater than 5 Ohms at 250 volts	
		o Isolation Meg Ohms: not less than 10 Mega Ohms	
		то:	Lev
		4.5.1.1 Test Criteria	
		4.5.1.1 Use this criteria when electrical testing is required.	
		o IPC 9252A Test Level C (Class 3)	
		o 100% Electrical net testing.	
		o Isolation Meg Ohms: not less than 10 Mega Ohms	
		o Continuity Testing Ohms (Normal): not greater than 10 Ohms at 40volts. Supplier may alternatively or voluntarily test up to 250volts at their discretion.	
		o High Voltage Continuity Testing (Special): if high voltage testing specified on drawing, test is to be performed at 10 ohms 250 volts.	
		o Isolation Meg Ohms: not less than 10 Mega Ohms	
		5.1.2.2 Add	
		"5.1.2.2 Small Parts	
	2	When area to be marked is less than 2" in length, the following options are permissible.	
<u>``</u>	$\mathcal{C}$	o It is permissible to spread part numbering and revision across multiple lines to accommodate tooling, or physical area of part.	
$\mathbf{V}$		o It is permissible to mark only "Rev" followed by the revision number / letter.	
		o It is permissible to mark only the revision number / letter	
		o It is permissible to shrink the text size such that	

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Revision		Change	Date
		magnification no greater than 4x is required for human inspection."	λ
		5.1.2.3 Add sentence "IFE may accept new technologies not on this list"	
-	First	-	12/14/2016
	Release		
A	Panel Sizes	<ul><li>4.49- Add edge plating section</li><li>4.5- Insert new section on preferred PCB</li></ul>	5/15/18
		fabrication panel dimensions.	
		4.5.1 – CAD Submittal, deadline and acceptable file types	
		4.5.4 – New Mouse Bite Specs	
		4.5.5 – New V-Score Specs	

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